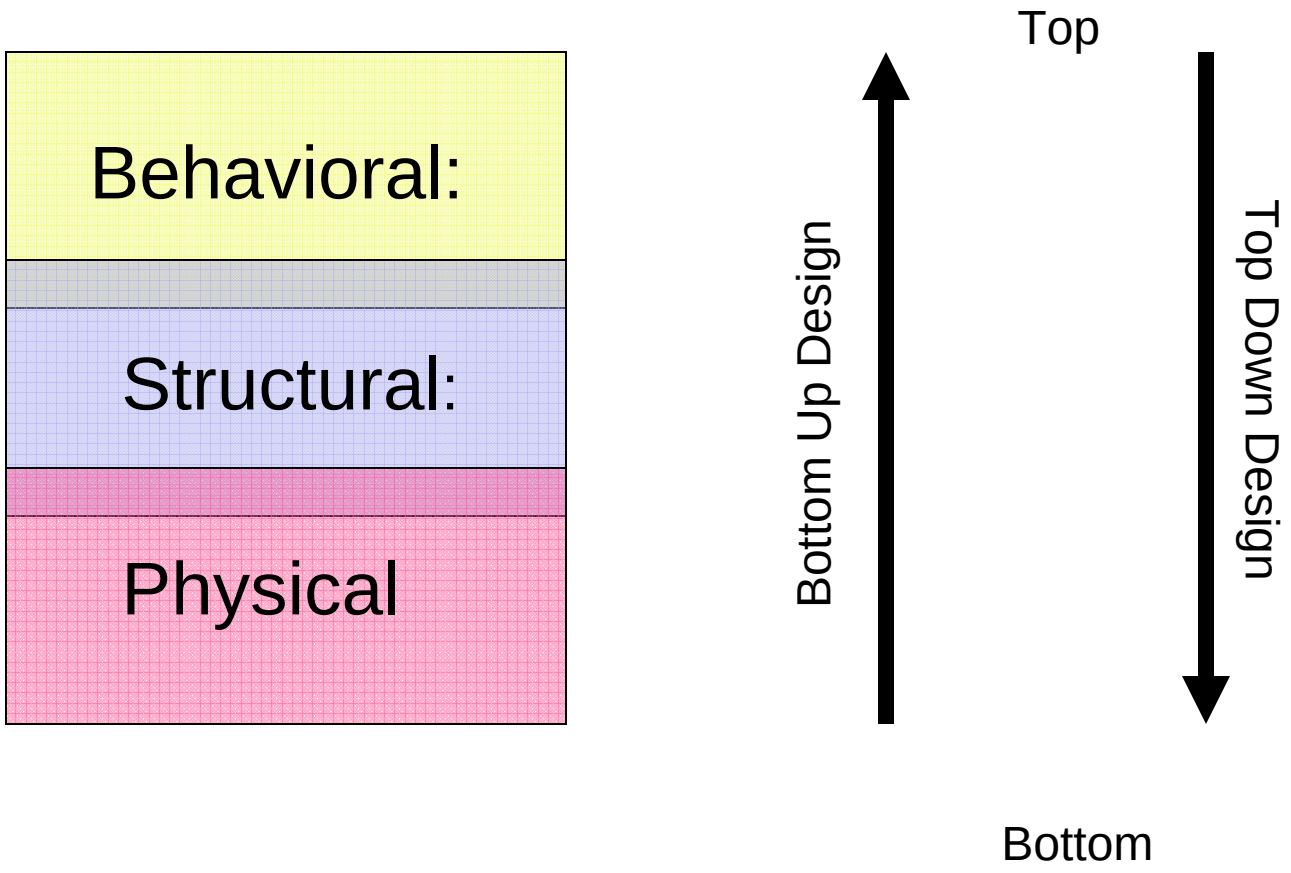
EE 434

Lecture 30

Logic Design

Review from last time:

Hierarchical Analog Design Domains:



Review from last time:

Hierarchical Digital Design Domains:

Behavioral : Describes what a system does or what it should do

Structural : Identifies constituent blocks and describes how these blocks are interconnected and how they interact

Physical : Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

Multiple representations often exist at any level or sublevel

Review from last time:

Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description
   - Technology independent
2. RTL Description

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer

5. Logic Synthesis

   Generally use a standard call library for synthesis

Review from last time:

6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   - DRC
   - Back Annotation
8. Post Layout simulation

   May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles

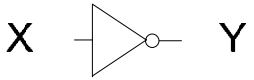
Logic Circuit Block Design

Many different logic design styles

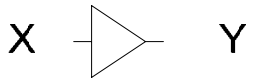
- Static Logic Gates
- Complex Logic Gates
- Pseudo NMOS
- Pass Transistor Logic
- Dynamic Logic Gates
  - Domino Logic
  - Zipper Logic
  - Output Prediction Logic

Various logic design styles often combined in the implementation of one logic block

The basic logic gates



$$Y = \overline{X}$$



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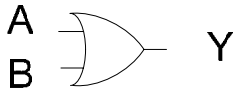

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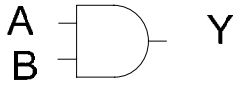

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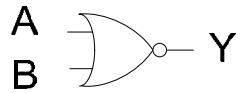

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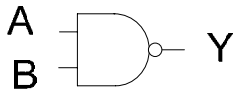

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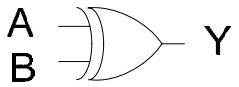

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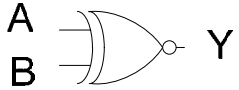

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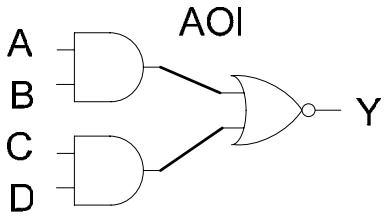
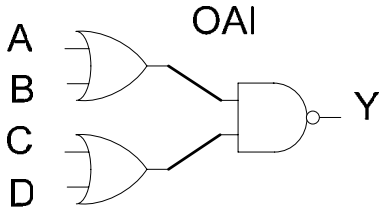
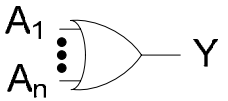


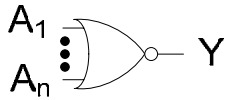
$$Y = \overline{A \bullet B + C \bullet D}$$



$$Y = \overline{(A + B) \bullet (C + D)}$$



$$Y = A_1 + A_2 + \ldots A_n$$



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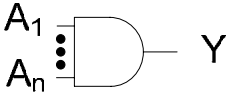

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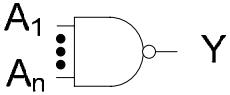

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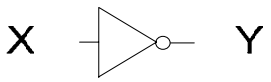
The basic logic gates



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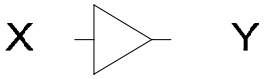

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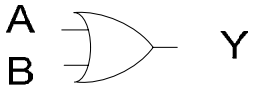

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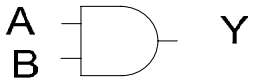

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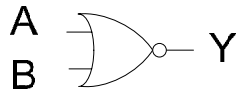

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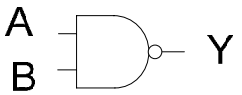

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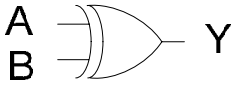

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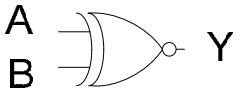


$$Y = \overline{A \oplus B}$$

Question: How many basic one and two input gates exist and how many of these are useful?

The basic logic gates

The set of NOR gates is complete

Any combinational logic function can be realized with only multiple-input NOR gates

The set of NAND gates is complete

Any combinational logic function can be realized with only multiple-input NOR gates

Performance of the BASIC gates is critical!

The basic logic gates

A gate logic family can be formed based upon a specific design style for implementing logic functions

Many different gate logic family types exist

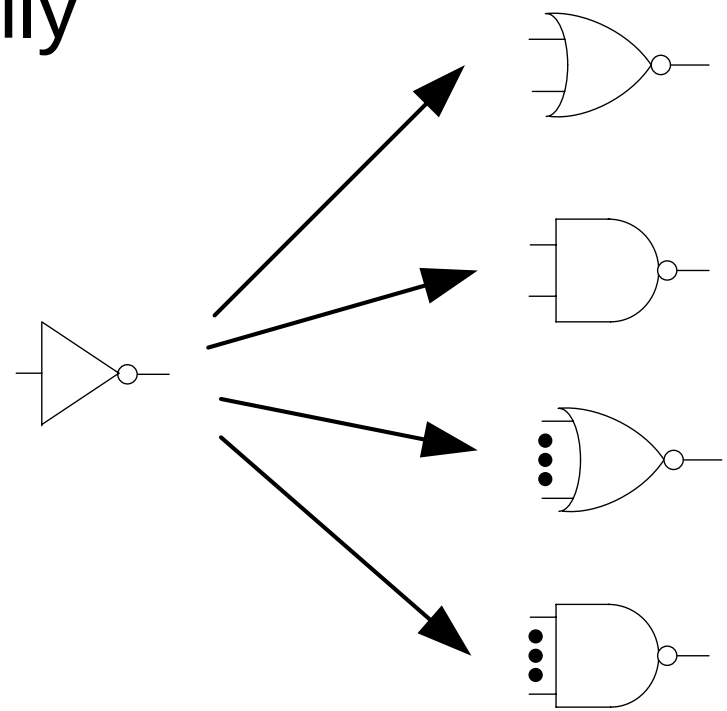
NMOS, PMOS, CMOS, TTL, ECL, RTL, DCTL,…

Substantial differences in performance from one family type to another

Power, Area, Noise Margins, ….

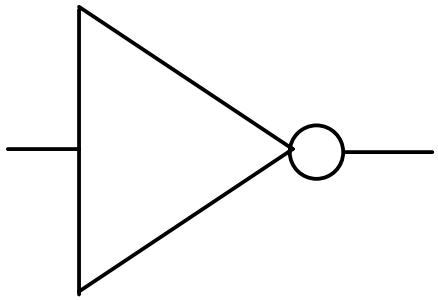
The basic logic gates

The characteristics of any gate logic family can be expressed rather simply in terms of the characteristics of the basic inverter in that logic family



The basic logic gates

It suffices to inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.



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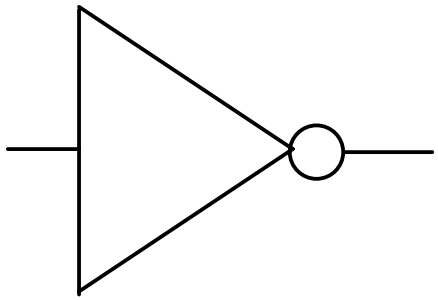

What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements

Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools

Are some of these more important than others?

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Yes ! – must have well-defined logic levels for circuits to even function as logic

Desirable and/or Required Logic Family Characteristics

Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

What properties of an inverter are necessary for it to be useful for building a logic family

What are the logic levels for a given inverter of for a given logic family?

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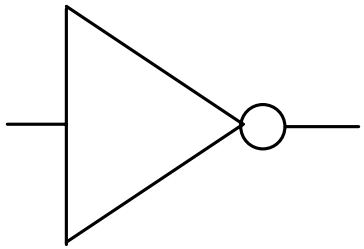
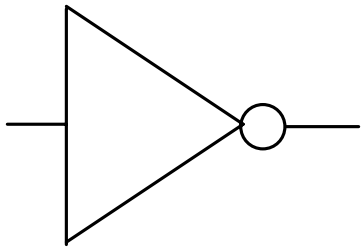


V_H=? V_L=?

Can we legislate them ?

- Some authors choose to simply define a value for them
- Simple and straightforward approach
- But what if the circuit does not interpret them the same way they are defined !!

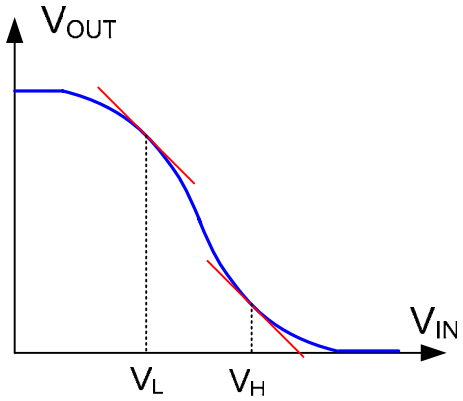
What are the logic levels for a given inverter of for a given logic family?



V_H=? V_L=?

Can we legislate them ?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined !!



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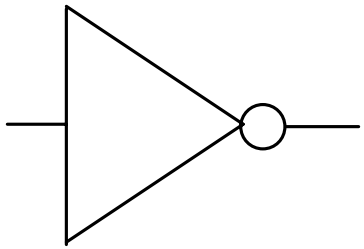
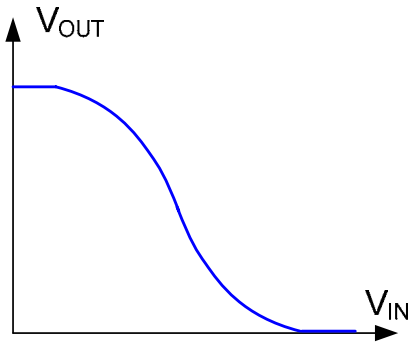


V_H=? V_L=?

Ask the inverter how it will interpret logic levels

- The circuit will interpret them the way they are defined !!
- Analytical expressions may be complicated
- How is this determination made?



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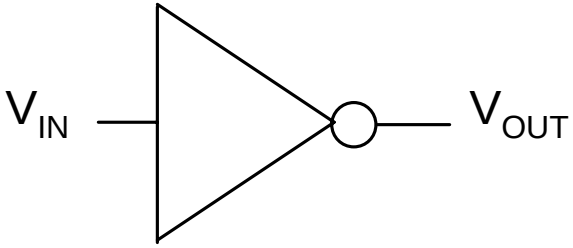

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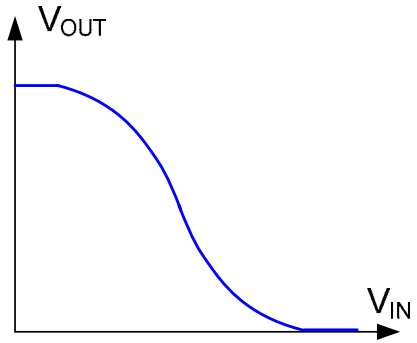

Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated